## Features

- Single 2.7V - 3.6V Supply
- Fast Read Access Time – 200 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10 ms Maximum
  - 1- to 64-byte Page Write Operation
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{Data}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- JEDEC Approved Byte-wide Pinout
- Industrial Temperature Ranges
- Green (Pb/Halide-free) Packaging Option

# 256K (32K x 8) Battery-Voltage Parallel EEPROMs

# AT28BV256

## 1. Description

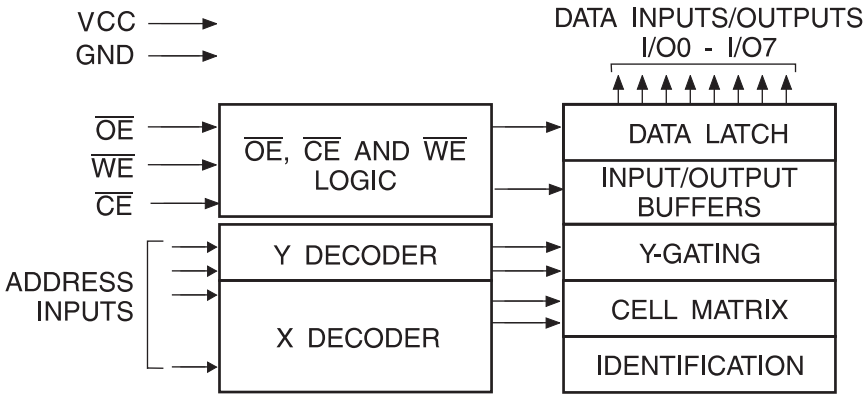
The AT28BV256 is a high-performance electrically erasable and programmable read-only memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 54 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

The AT28BV256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{Data}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's AT28BV256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

0273J–PEEPR–10/06

## 3. Block Diagram




## 4. Absolute Maximum Ratings*

| | |
|---|---|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to $V_{CC}$ + 0.6V |
| Voltage on $\overline{OE}$ and A9 with Respect to Ground | -0.6V to +13.5V |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## 6. DC and AC Operating Range

| | AT28BV256-20 |
|---|---|
| Operating Temperature (Case) | -40°C - 85°C |
| $V_{CC}$ Power Supply | 2.7V - 3.6V |

## 7. Operating Modes

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O |
|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ |
| Write[2] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ |
| Standby/Write Inhibit | $V_{IH}$ | X[1] | X | High Z |
| Write Inhibit | X | X | $V_{IH}$ | |
| Write Inhibit | X | $V_{IL}$ | X | |
| Output Disable | X | $V_{IH}$ | X | High Z |
| Chip Erase | $V_{IL}$ | $V_H$[3] | $V_{IL}$ | High Z |

Notes: 1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to AC programming waveforms.
3. $V_H$ = 12.0V ± 0.5V.

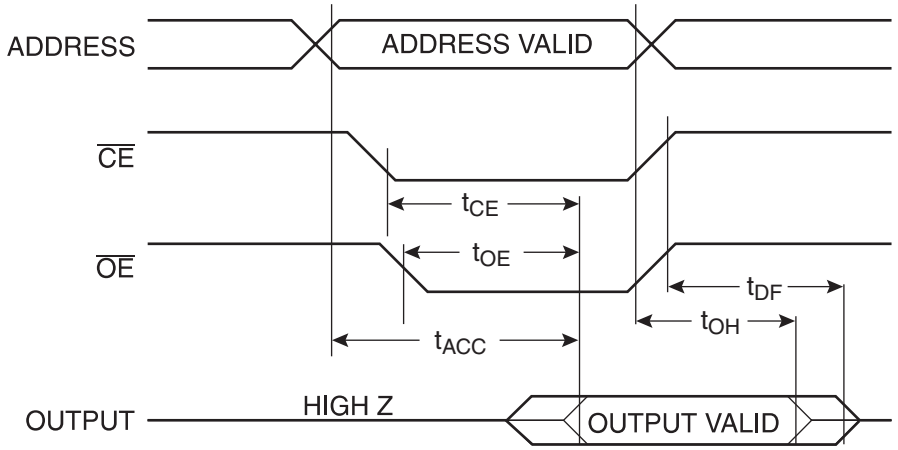
## 8. DC Characteristics

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ + 1V | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{I/O}$ = 0V to $V_{CC}$ | | 10 | µA |
| $I_{SB}$ | $V_{CC}$ Standby Current CMOS | $\overline{CE}$ = $V_{CC}$ - 0.3V to $V_{CC}$ + 1V | | 50 | µA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz; $I_{OUT}$ = 0 mA | | 15 | mA |
| $V_{IL}$ | Input Low Voltage | | | 0.6 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1.6 mA | | 0.3 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -100 µA | 2.0 | | V |

## 9. AC Read Characteristics

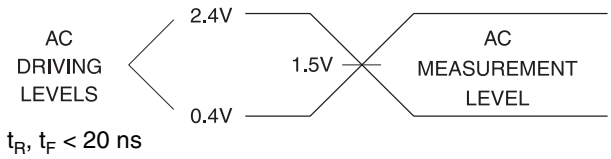
| Symbol | Parameter | AT28BV256-20 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | | 200 | ns |
| $t_{CE}$[1] | $\overline{CE}$ to Output Delay | | 200 | ns |
| $t_{OE}$[2] | $\overline{OE}$ to Output Delay | 0 | 80 | ns |
| $t_{DF}$[3][4] | $\overline{CE}$ or $\overline{OE}$ to Output Float | 0 | 55 | ns |
| $t_{OH}$ | Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first | 0 | | ns |

## 10. AC Read Waveforms[1][2][3][4]



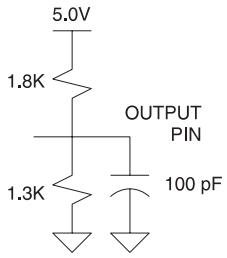

Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on $t_{ACC}$.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$ or by $t_{ACC} - t_{OE}$ after an address change without impact on $t_{ACC}$.
3. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L$ = 5 pF).
4. This parameter is characterized and is not 100% tested.

## 11. Input Test Waveforms and Measurement Level




$t_R$, $t_F$ < 20 ns

## 12. Output Test Load




## 13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

| Symbol | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 6 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: 1. This parameter is characterized and is not 100% tested.

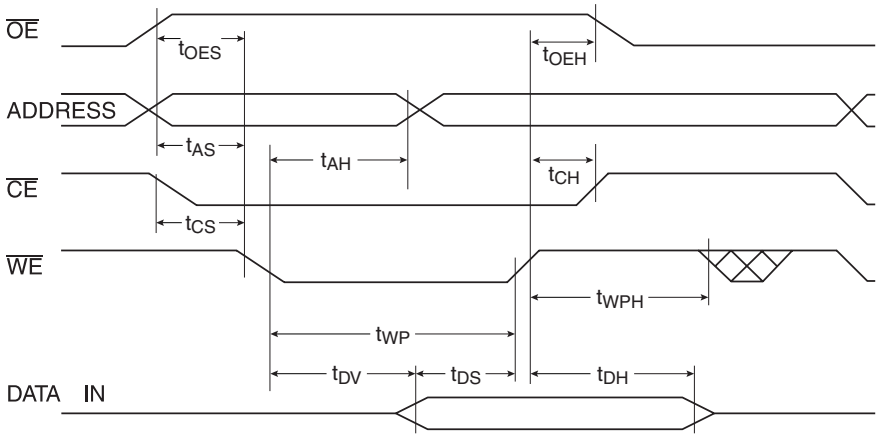
## 14. AC Write Characteristics

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AS}$, $t_{OES}$ | Address, $\overline{OE}$ Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{CS}$ | Chip Select Set-up Time | 0 | | ns |
| $t_{CH}$ | Chip Select Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width ($\overline{WE}$ or $\overline{CE}$) | 200 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | ns |
| $t_{DH}$, $t_{OEH}$ | Data, $\overline{OE}$ Hold Time | 0 | | ns |
| $t_{DV}$ | Time to Data Valid | NR[1] | | |

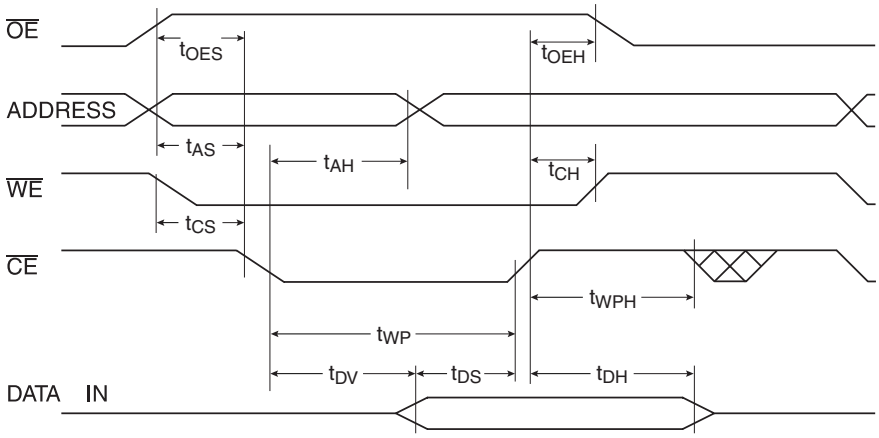
Note: 1. NR = No Restriction.

## 15. AC Write Waveforms

### 15.1 $\overline{WE}$ Controlled



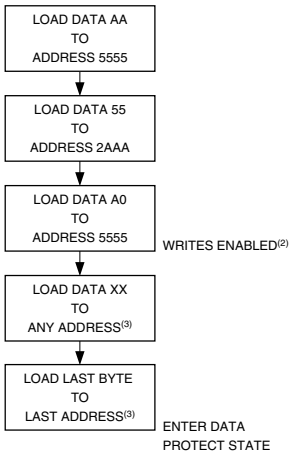

### 15.2 $\overline{CE}$ Controlled



## 16. Page Mode Characteristics

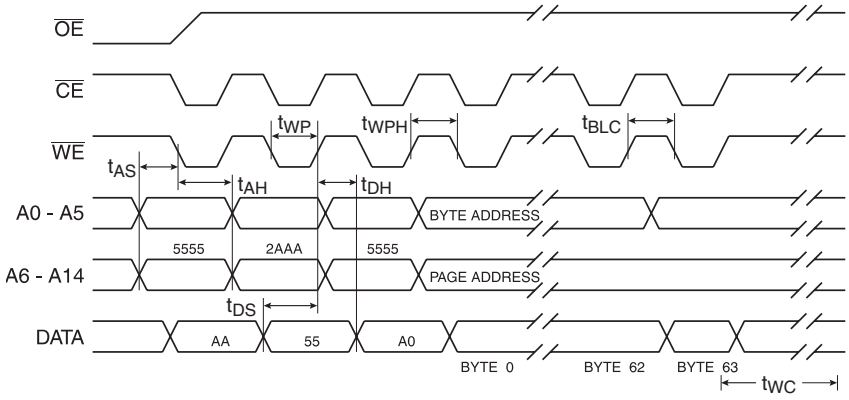
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | | 10 | ms |
| $t_{AS}$ | Address Set-up Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{DS}$ | Data Set-up Time | 50 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 200 | | ns |
| $t_{BLC}$ | Byte Load Cycle Time | | 150 | µs |
| $t_{WPH}$ | Write Pulse Width High | 100 | | ns |

## 17. Programming Algorithm(1)(2)(3)




Notes:
1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).
2. Data protect state will be re-activated at the end of program cycle.
3. 1 to 64 bytes of data are loaded.

## 18. Software Protected Program Cycle Waveforms(1)(2)(3)




Notes:
1. A0 - A14 must conform to the addressing sequence for the first three bytes as shown above.
2. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

# 24. Ordering Information

## 25. Standard Package

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 200 | 15 | 0.02 | AT28BV256-20JI<br>AT28BV256-20PI<br>AT28BV256-20SI<br>AT28BV256-20TI | 32J<br>28P6<br>28S<br>28T | Industrial<br>(-40° to 85° C) |

Note: 1. See Valid Part Numbers table below.

## 26. Green Package Option (Pb/Halide-free)

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 200 | 15 | 0.02 | AT28BV256-20JU<br>AT28BV256-20TU<br>AT28BV256-20SU<br>AT28BV256-20PU | 32J<br>28T<br>27S<br>28T | Industrial<br>(-40° to 85° C) |

# 27. Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

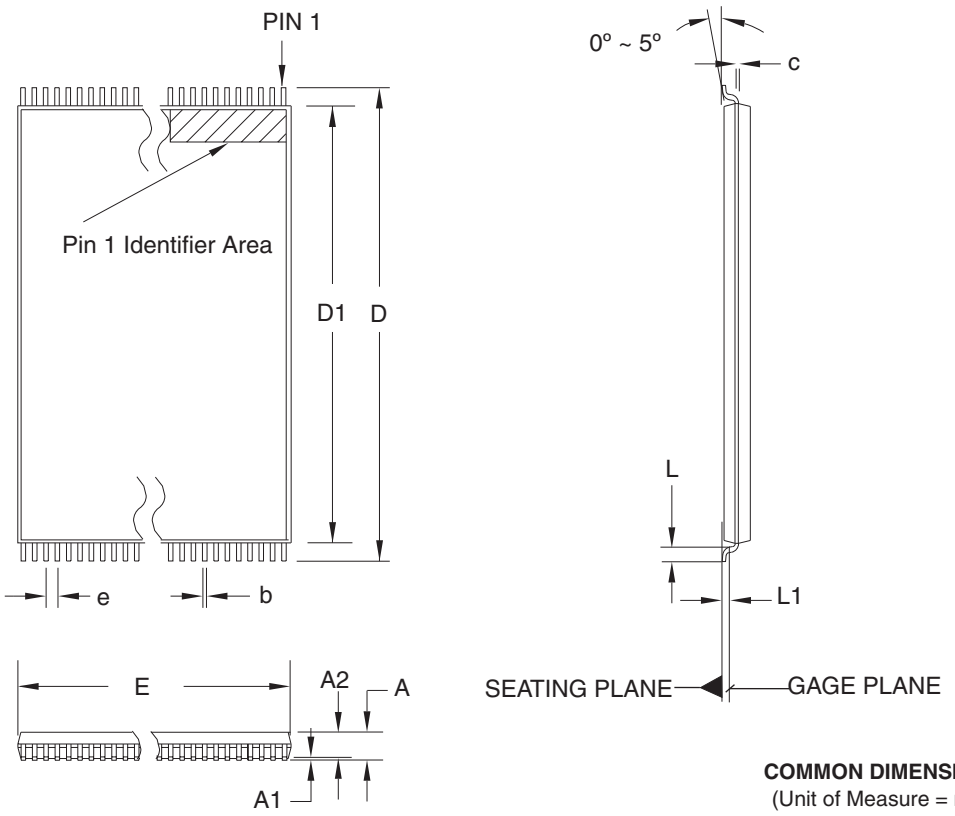
| Device Numbers | Speed | Package and Temperature Combinations |
|---|---|---|
| **AT28BV256** | 20 | JI, PI, SI, TI, TU, JU, SU, PU |

# 28. Die Products

| Reference Section: Parallel EEPROM Die Products |
|---|

| Package Type | |
|---|---|
| **32J** | 32-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **28P6** | 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **28S** | 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| **28T** | 28-lead, Plastic Thin Small Outline Package (TSOP) |

## 29.4 28T – TSOP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.90 | 1.00 | 1.05 | |
| D | 13.20 | 13.40 | 13.60 | |
| D1 | 11.70 | 11.80 | 11.90 | Note 2 |
| E | 7.90 | 8.00 | 8.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.55 BASIC | | | |

Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP) | 28T | C |